

**TEMPORARY DEVICE ATTACH STRUCTURE FOR TEST AND BURN IN OF
MICROJOINT INTERCONNECTS AND METHOD FOR FABRICATING THE SAME**

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FIELD OF THE INVENTION

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This invention pertains to the field of microelectronics and, more particularly, to the field of fabricating and interconnecting extremely small semi-conductor devices commonly referred to as "chips."

RELATED INVENTIONS

The present invention is related to certain inventions assigned to the assignee of the present invention. These are in co-pending applications YOR920010217US1 and 20010216US1, the disclosures of which are cross-referenced and incorporated herein.

BACKGROUND OF THE INVENTION

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Increased levels of integration in the silicon transistor technology over the last two decades have facilitated the migration from large scale integrated (LSI) to very large scale integrated (VLSI) and now to ultra-large scale integrated (ULSI) circuits for use in silicon chips for computing, communication and micro controller applications. Optimum utilization of these highly integrated silicon chips requires a more space efficient packaging with supporting devices such as memory chips. Further, with the advent of mobile communication devices, hand held organizers and computing devices, there has also been a push to integrate such varied functions into a single compact system. This in turn has led to the push in the microelectronics industry towards system-on-a-chip (SOC) approach.

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Simply stated, the SOC approach attempts to integrate as many of these different device functionalities on the same silicon chip so that a single large chip can provide a variety of functions to the end user. Although conceptually very attractive such an approach is practically daunting due to several reasons. First, the materials, fabrication processes and feature sizes optimum for the different microelectronic devices (such as memory chips, logic chips, wireless communication chips, etc.) are quite different from each other. Combining them all onto the same chip implies making compromises that can limit the performance achievable in each of the

device blocks in the SOC. Second, integration of a large number of functional blocks requires a large chip size with many levels of wiring constructed on the chip. Both these factors tend to reduce the yield and increase the cost per chip, which is undesirable. Third, one has to design and build every unique combination of functions (e.g., memory and microprocessor, wireless communication and microprocessor, etc.) leading to a large variety of chip part numbers and product mix that is not conducive to low cost reduced manufacturing. Last, the expertise required for combining a diverse set of materials, process and integration schemes on a single SOC is often not available in a single enterprise as these are currently part of different microelectronic businesses.

An attractive alternative to SOC is system-on-a-package or SOP wherein a number of chips, each optimized for its unique function and perhaps manufactured in different factories specially tailored to produce the specific chips are combined on a first level packaging carrier that interconnects them and allows the resulting package to function as a single system. The level of interconnection and input-output- (I/O) density required in such a package is expected to be far greater than those currently available in printed circuit board or multilayer ceramic technologies. Since this SOP carrier with chips assembled on it is expected to replace an SOC, it is reasonable to expect that the interconnect and I/O densities should be somewhere between those used in the far back end of the line (FBEOL) interconnect levels on chips (typically wiring and vias on 500nm to 1000nm pitch) and the most aggressive packaging substrates (typically vias and wiring on 10,000 to 20,000nm pitch). Extension of the FBEOL processes at the required wiring size and pitch for the SOP carrier is feasible if the carrier itself is made of silicon. In addition, however, the carrier would be required to support a high I/O density in order to interconnect the various device chips mounted on it. Greater the granularity of the system, that is, finer the division of the system into sub-units or chips, greater will be the number of I/Os required. It is expected that such I/O densities will necessitate bonding pads that are on the order of 5 to 10 μ m size and spaces which are presently outside the realm of possibility of typical packaging I/O pads which are at least 10 to 20 times coarser in size and spacing.

It is therefore highly desirable to enable a microjoining structure to interconnect several chips on to a system-on-a-package carrier to achieve significantly higher input/output density between the chips as compared to the current state-of-the-art.

Concomitantly, a particular need has arisen for temporarily – rather than permanently -- interconnecting a collection of devices such as chips involving a high density array of the aforesaid microjoints for the specific purpose of first performing a system-level test and then for

performing a "burn in." This enables one to sort out and combine the good quality chips on to the carrier to form a functional and reliable system on a package.

SUMMARY OF THE INVENTION

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A general object of the present invention is to furnish the ability to test and "burn in" device chips that require ultra high pitch I/O pads (down to approximately 2.5 μ m on 5 μ m centers).

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Another object of the present invention is to realize the ability to test devices that are to be tested and burned in as a part of a collection of devices that form a functional system.

The ability to do all of the above is achieved without forming a permanent metallurgical joint to the devices. This eliminates the need to apply forces to the microjoints to remove bad chips from the test substrate, which is particularly important for these very small sized joint structures.

The test carrier of this invention is reusable for many test cycles since no permanent bonds are formed with the parts that are tested on it. A sorting of the devices that have been tested is carried out based on their level of performance under the test conditions, and particularly is based on a suitable metric (e.g. device speed at the system level).

In fulfillment of the above stated objects, and the particular need noted that has arisen in this art, the present invention, briefly stated, provides a structure comprising a system level test and burn in carrier, said structure comprising: a system for testing an array of device chips by temporarily attaching a microjoint structure, comprising a carrier, to the array, the carrier being a multilayer substrate having a plurality of receptacles provided with microdendritic surface features, said receptacles matching a pattern and size of microjoint pads on the device chips; test pads; interconnect wiring that connects the test pads to the microdendritic receptacle array, and interconnect wiring additionally providing connections between a multiplicity of the devices mounted on the carrier so as to form a complex functional system that can be adequately tested while on the carrier.

In accordance with the process of the present invention, the device chips to be tested and burned in are provided with microjoint connection metallurgies according to related dockets YOR...0216 and YOR...0217. Then with application of a conformal pressure the device pads

are pushed against the microdendritic contacts on the carrier so as to establish a reliable temporary electrical connection for the duration and conditions of a typical test and burn in process. At the end of this regimen, any bad quality chips are removed and replaced with new chips. The regimen iteratively leads to a final collection of chips deemed to be functional at a system level with a good degree of reliability.

The foregoing and still further objects and advantages of the present invention will be more apparent from the following detailed explanation of the preferred embodiments of the invention in connection with the accompanying drawing.

DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a carrier with metal depositions over a contact receptacle that was formed in an earlier deposited dielectric film.

Figure 2 shows the carrier after removal of the metal, in the form of copper, from the surface by chemical mechanical polishing (CMP) and deposition of a nickel layer and Pd dendrites.

Figure 3 depicts the carrier after etching of the TaN-Ta layer above the dielectric, and showing temporary joining of a stud extending from a device chip.

DESCRIPTION OF PREFERRED EMBODIMENT

It will become apparent as description of the invention proceeds that because the aforementioned objects are fulfilled there is an ability, according to the invention, to test devices that have to be tested and "burned in" as a part of a collection of devices that form a functional system (e.g., electro/optical system, network switching systems, a multiprocessor parallel computing systems) thereby to ensure system level operability and performance. Consequently, this allows a selection of a group of chips that are known to be good as a group; alternately, the method of the invention allows a sorting of a particular part or chip that is prone to low yield or varying levels of performance by testing a number of chips mounted on the test carrier along with a known good collection of other chips that make up the full system. When the testing is completed the temporarily attached device chips can be separated from the test carrier.

It will be understood that when one begins the fabrication method in accordance with the present invention, one starts with the carrier component 10 constituted of the material 12, such as silicon, ceramic or organic carrier, with the interchip wiring 16. Wiring of contacts to connect to external electronics must be carried out. The wiring will have multiple levels and the carrier will also have vias, not shown on Figure 1, but extending through the carrier 10 to allow for connections to the back of the carrier.

It will be seen that the representative receptacle 20, as seen in Figure 1, extends into the dielectric layer 14 where contacts to the device chips are made with respect to a representative device wafer 30 with a representative stud 32 extending from it and having a metal tip 34 (Figure 3). The important point to note is that the size of the receptacles 20 can be as small as about 2.5 microns. The size of the receptacle, additionally, is about 20% larger than the size of the stud 32.

It will further be seen in Figure 1 that a liner/seed layer 22 is deposited, which is usually constituted of 0.04 micron layers of TaN-Ta, as well as a 0.1 micron Cu layer 24.

After the layers 22 and 24 have been deposited the copper layer is polished off by the use of chemical mechanical polishing (CMP) from the top surface stopping on the layer 22 of TaN-Ta. Cu is left in the bottom of the contact receptacles and on their sidewalls.

The next step in the method is the electroplating of a 0.5 micron layer 26 of a barrier such as nickel into the contact openings, using a process that plates only on Cu. The TaN-Ta serves to bring in the current, but no plating takes place there.

Next, a three-step technique is used to electroplate a base strike layer of Pd, a dendritic layer of Pd and a reinforcing over-layer of Pd. All of these Pd layers are designated 28. Different plating solution concentrations, current densities, and/or ultrasonic agitation levels will be used to achieve the dendritic Pd triple layer. Optionally, the dendrites can be made of a non-noble metal such as Ni or Cu and plated over with a noble metal such as Pd, Pt or Rh.

Etching is now performed to remove the TaN-Ta layer 22 from the region between the receptacles, the result thereof being depicted in Figure 3. Chemical or dry plasma etching can be used for this step. The finished carrier structure 10 (Figure 3) now has female receptacles 20 populated with noble metal asperities that will engage and penetrate into the softer microjoint solder or Au-Sn tipped pads 34 on the device chip studs 32 when the test carrier and the chip 30 are aligned and assembled together under a conformal back pressure assembly not shown in

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